What is claimed is:

1. A method for controlling a central processing unit for addressing in relation to a memory, wherein a set of operation code identifiers including at least one special operation code identifier is associated to the central processing unit, wherein the central processing unit is arranged to address a first memory area having a first memory size of the memory, wherein the method comprises the following steps:

monitoring a data traffic from the memory to the central processing unit by supporting means coupled to the central processing unit;

in the case in which the data traffic from the memory to the central processing unit includes the special operation code identifier,

forming a new address by the supporting means, wherein the new address is defined in a second memory area having a second memory size of the memory, wherein the second memory size is larger than the first memory size;

providing a predetermined operation code identifier to which a jump command from a command set of the central processing unit is assigned, to the central processing unit by the supporting means, wherein the predetermined operation code identifier has a destination address in relation to the first memory area; and

managing a code descriptor by the supporting means, yielding, together with the destination address, the new address.

2. A controller having:

a central processing unit having a set of operation code identifiers including at least one special operation code identifier, wherein the central processing unit is arranged to address a first memory area having a first memory size of a memory;

supporting means coupled to the central processing unit to monitor a data traffic from the memory to the central processing unit,

wherein the supporting means is arranged to perform, in the case in which the data traffic from the memory to the central processing unit includes the special operation code identifier, the following steps:

forming a new address, wherein the new address is defined in a second memory area having a second memory size of the memory, wherein the second memory area is larger than the first memory area, and

providing a predetermined operation code identifier to which a jump command from a command set of the central processing unit is assigned, to the central processing unit, wherein the predetermined operation code identifier has a destination address in relation to the first memory area; and

managing a code descriptor, yielding, together with the destination address, the new address.

3. The controller according to claim 2, wherein the set of operation code identifiers comprises a plurality of operation code identifiers, to which commands are associated determining the command set of the central processing unit, and wherein no command from the command set of the central processing unit is assigned to the special operation code identifier.

4. The controller according to claim 2, further comprising:

an external register for storing the code descriptor, wherein the external register is arranged externally of the central processing unit, wherein the code descriptor is provided to define the position of the first memory area within the second memory area,

wherein the supporting means is arranged to perform, in the case that the data traffic from the memory to the central processing unit includes the special operation code identifier, the following steps:

setting a value of the code descriptor in such a way that the new address is contained in the first memory area, and

setting the destination address in relation to the first memory area in such a way that the destination address in relation to the first memory area corresponds to the new address in relation to the second memory area.

5. The controller according to claim 4, further comprising:

a program counter included in the central processing unit, in which a code address in relation to the first memory area is stored;

means coupled to the central processing unit in order to monitor a data traffic from the central processing unit to the memory, and arranged to perform, in the case that the data traffic from the central processing unit to the memory includes the code address in relation to the first memory area, the following steps:

manipulating it based on the contents of the code descriptor to obtain the new address in relation to the second memory area; and

passing it on to the memory in a changed form in order to access the memory.

6. The controller according to claim 2, wherein the central processing unit is arranged to perform, responsive to the supplied predetermined operation code identifier for requesting a next operation code identifier to be processed, the following steps:

storing the destination address in a program counter of the central processing unit, and

outputting it within the data traffic from the central processing unit to the memory.

7. The controller according to claim 2, wherein the central processing unit further comprises a stack memory and a stack memory pointer indicating a position in the stack memory where data is currently taken from the stack memory by the central processing unit or added to it, and wherein the supporting means is adapted to further provide at least another predetermined operation code identifier to the central processing unit, wherein a command from the command set of the central processing unit for filling the stack memory at the stack memory pointer with a value depending on a current address in relation to the second memory area at which the operation code identifier following the special operation code identifier is arranged is assigned to the at least one further operation code identifier.

8. The controller according to claim 2, wherein the destination address is a less significant part of the new address and the descriptor is a more significant part of the new address.

9. A method for controlling a central processing unit for addressing in relation to a memory, wherein a set of operation code identifiers including at least a special operation code identifier is associated to the central processing unit, wherein the central processing unit is arranged to address a first memory area having a first memory size of the memory, wherein the method comprises the following steps:

monitoring a data traffic from the memory to the central processing unit and a data traffic from the central processing unit to the memory by supporting means coupled to the central processing unit;

if the data traffic from the memory to the central processing unit includes the special operation code identifier,

forming a new address by the supporting means, wherein the new address is defined in a second memory area having a second memory size of the memory, wherein the second memory size is larger than the first memory size;

providing a predetermined operation code identifier to which a command from the command set of the central processing unit is assigned, to the central processing unit by the supporting means; and

manipulating an address defined in relation to the first memory area, within the data traffic from the central processing unit to the memory based on the new address by the supporting means in order to obtain a manipulated address in relation to the second memory area.

10. A controller having:

a central processing unit having a set of operation code identifiers including at least a special operation code identifier, wherein the central processing unit is arranged to address a first memory area having a first memory size of a memory;

supporting means coupled to the central processing unit in order to monitor a data traffic from the memory to the central processing unit and a data traffic from the central processing unit to the memory,

wherein the supporting means is arranged to perform, in the case that the data traffic from the memory to the central processing unit includes the special operation code identifier, the following steps:

forming a new address, wherein the new address is defined in a second memory area having a second memory size of the memory, wherein the second memory size is larger than the first memory size;

providing a predetermined operation code identifier to which a command from the command set of the central processing unit is associated, to the central processing unit; and

manipulating an address defined in relation to the first memory area, within the data traffic from the central processing unit to the memory based on the new address in order to obtain a manipulated address in relation to the second memory area.

11. The controller according to claim 10, wherein the set of operation code identifiers comprises a plurality of operation code identifiers to which commands are assigned determining the command set of the central processing unit,

and wherein no command from the command set of the central processing unit is associated to the special operation code identifier.

12. The controller according to claim 10, wherein the predetermined operation code identifier is associated to a write or read command from the command set of the central processing unit.

13. The controller according to claim 10, wherein the command relates to an access address in relation to the first memory area corresponding to a portion of the new address, and wherein the supporting means is arranged to perform, when manipulating the address defined in relation to the first memory area within the data traffic from the central processing unit to the memory, the following step:

supplementing it by a remaining portion of the new address.

14. The controller according to claim 10, wherein the command relates to an access address in relation to the first memory area, and wherein the supporting means is arranged to perform, when manipulating the address defined in relation to the first memory area within the data traffic from the central processing unit to the memory, the following step:

replacing it by the new address.

15. The controller according to claim 13, wherein the command further relates to an offset value, and wherein the supporting means is arranged to add the offset value to the manipulated address.

16. The controller according to claim 10, further comprising:

an external register for storing an address, wherein the external register is arranged externally of the central processing unit, wherein this address is provided to indicate a position of the first memory area within the second memory area;

means coupled to the central processing unit to monitor the data traffic from the central processing unit to the memory and arranged to perform, in the case that the data traffic from the central processing unit to the memory includes an address defined in relation to the first memory area, the following steps:

manipulating it based on the contents of the external register to obtain a corresponding address in relation to the second memory area, and

passing it on to the memory in a changed form to access the memory,

and wherein the supporting means is arranged to perform, in the case that the data traffic from the memory to the central processing unit includes the special operation code identifier, the following step:

adapting the contents of the external register in such a way that the first memory area contains the manipulated address,

and in the case that the data traffic from the memory to the central processing unit includes an operation code identifier of the plurality of operation code identifiers, to which a read or write command from the command set of the central processing unit is associated, to perform the following steps:

passing it on to the central processing unit, and

leaving unchanged the address defined in relation to the first memory area, in the data traffic from the central processing unit to the memory.

17. The controller according to claim 10, wherein the special operation code identifier corresponds to a command for handling a generic pointer, wherein the generic pointer consists of an address indication and an addressing type indication, wherein the address indication corresponds to the new address, and wherein the addressing type indication indicates that the address indication refers to the second memory area.

18. The controller according to claim 17, wherein the supporting means is arranged to perform, in the case in which the data traffic from the memory to the central processing unit includes a special operation code identifier corresponding to a command for handling a generic pointer consisting of an address indication and an addressing type indication, the following steps:

checking the addressing type indication,

in the case that the addressing type indication indicates that the address indication refers to the second memory area, performing the formation of the new address, the supply of the predetermined operation code identifier and the manipulation of the address, and

in the case that the addressing type indication indicates that the address indication refers to the first memory area, supplying the central processing unit with an operation code identifier to which a command from the command set referring to the address indication is associated.

19. The controller according to claim 2, wherein the central processing unit comprises at least an internal

register and the supporting means is coupled to the central processing unit to determine the contents of the at least one internal register, and arranged to perform the following steps when forming the new address:

determining the contents of the at least one internal register, and

forming the new address from the contents of the at least one internal register.

20. The controller according to claim 10, wherein the central processing unit comprises at least an internal register and the supporting means is coupled to the central processing unit to determine the contents of the at least one internal register, and arranged to perform the following steps when forming the new address:

determining the contents of the at least one internal register, and

forming the new address from the contents of the at least one internal register.

21. The controller according to claim 2, comprising at least one external data pointer register arranged externally of the central processing unit, and wherein the supporting means is arranged to perform the following steps when forming the new address:

determining the contents of the at least one external data pointer register, and

forming the new address from the contents of the at least one external data pointer register.

22. The controller according to claim 10, comprising at least one external data pointer register arranged

externally of the central processing unit, and wherein the supporting means is arranged to perform the following steps when forming the new address:

determining the contents of the at least one external data pointer register, and

forming the new address from the contents of the at least one external data pointer register.

23. The controller according to claim 2, wherein the supporting means is arranged to perform the following step when forming the new address:

forming the new address at least partly from an address portion of the operation code identifier.

24. The controller according to claim 10, wherein the supporting means is arranged to perform the following step when forming the new address:

forming the new address at least partly from an address portion of the operation code identifier.

25. The controller according to claim 23, wherein the supporting means is arranged to perform the following step when forming the new address at least partly from the address portion of the operation code identifier:

providing the central processing unit with the or another special operation code identifier, and

wherein the central processing unit comprises a program counter in which a code address in relation to the first memory area is stored, and the central processing unit is arranged to perform the following steps:

requesting a next operation code identifier to be processed by means of the code address, and

increasing the program counter responsive to the special operation code identifier supplied to the central processing unit and otherwise ignoring the special operation code identifier supplied to the central processing unit.

26. The controller according to claim 24, wherein the supporting means is arranged to perform the following step when forming the new address at least partly from the address portion of the operation code identifier:

providing the central processing unit with the or another special operation code identifier, and

wherein the central processing unit comprises a program counter in which a code address in relation to the first memory area is stored, and the central processing unit is arranged to perform the following steps:

requesting a next operation code identifier to be processed by means of the code address, and

increasing the program counter responsive to the special operation code identifier supplied to the central processing unit and otherwise ignoring the special operation code identifier supplied to the central processing unit.

27. The controller according to claim 2, wherein the supporting means is arranged to perform, in the case in which the special operation code identifier is included in the data traffic from the memory to the central processing unit, the following step:

stopping incoming interrupt signals.

28. The controller according to claim 10, wherein the supporting means is arranged to perform, in the case in which the special operation code identifier is included in the data traffic from the memory to the central processing unit, the following step:

stopping incoming interrupt signals.